WHAT IS CLAIMED IS (US) :

1. A decoder circuit, which is mounted on an integrated circuit, decoding an input voltage supplied to a single external input terminal into three or more control outputs,

the decoder circuit comprising:

a P-type transistor in which an emitter (source) is connected to a power source line of high level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a first control output; and

an N-type transistor in which an emitter (source) is connected to a power source line of low level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a second control output.

2. The decoder circuit according to claim 1, further comprising:

one or more voltage decreasing means of which one end is connected to the external input terminal; and

one or more first additional transistor in which a base (gate) is connected to the other end of the voltage decreasing means or to one of contacts of the voltage decreasing means, and an emitter (source) is connected to

the power source line of high level or low level, and a collector (drain) is an output terminal of a control output.

3. The decoder circuit according to claim 1, further comprising:

a first voltage-dividing circuit, standing between the external input terminal and the base (gate) of the P-type transistor, in which four or more voltage-dividing resistors are connected in series between the power source lines, the external input terminal is connected to a first contact of the voltage-dividing resistors, the base (gate) of the P-type transistor is connected via a bias resistor to a second contact of the voltage-dividing resistors, and the base (gate) of the N-type transistor is connected via a bias resistor to a third contact of the voltage-dividing resistors, the second contact having a voltage level higher than that of the first contact, the third contact having a voltage level lower than the first contact;

one or more first additional transistor in which a base (gate) is connected via a bias resistor to a contact having a voltage level lower than the first contact;

a second voltage-dividing circuit to which current taken in the P-type transistor is supplied; and

one or more second additional transistor in which a base (gate) is connected via a bias resistor to a contact of

voltage-dividing resistors of the second voltage-dividing circuit.

4. A photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a decoder circuit,

the decoder circuit, which is mounted on an integrated circuit, decoding an input voltage supplied to a single external input terminal into three or more control outputs,

the decoder circuit comprising:

a P-type transistor in which an emitter (source) is connected to a power source line of high level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a first control output; and

an N-type transistor in which an emitter (source) is connected to a power source line of low level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a second control output.

5. An optical pickup including a photo-detecting amplifier circuit for a disk recording/reproducing apparatus, being capable of switch function by means of a

decoder circuit,

the decoder circuit, which is mounted on an integrated circuit, decoding an input voltage supplied to a single external input terminal into three or more control outputs,

the decoder circuit comprising:

a P-type transistor in which an emitter (source) is connected to a power source line of high level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a first control output; and

an N-type transistor in which an emitter (source) is connected to a power source line of low level, a base (gate) is connected to the external input terminal, and a collector (drain) is an output terminal of a second control output.